## IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) For use with a clocked circuit, a clock selection circuit capable of receiving a first input clock signal and a second input clock signal and outputting to said clocked circuit a selected clock signal derived from one of said first and second input clock signals, said clock selection circuit comprising:

a first clock control circuit that receives said first input clock signal and a first start signal, wherein said first start signal, when asserted, is capable of causing said first clock control circuit to output a first gated clock signal;

a second clock control circuit that receives said second input clock signal and a second start signal, wherein said second start signal, when asserted, is capable of causing said second clock control circuit to output a second gated clock signal;

a first interlock circuit that detects when said first clock control circuit begins outputting said first gated clock signal and, in response to said detection, that asserts a first disable signal capable of preventing said second clock control circuit from outputting said second gated clock signal;

a second interlock circuit that detects when said second clock control circuit begins outputting said second gated clock signal and, in response to said detection, that asserts a second disable signal capable of preventing said first clock control circuit from outputting said first gated clock signal; and

a first OR gate that receives said first and second gate clock signal and outputs said selected clock signal;

wherein the first clock control circuit comprises a first flip-flop, a second flip-flop coupled in series with the first flip-flop, and a second OR gate having a first input coupled to an output of the first flip-flop and a second input coupled to an output of the second flip-flop.

2. (Original) The clock selection circuit as set forth in Claim 1 wherein said first interlock circuit detects when said first clock control circuit stops outputting said first gated clock signal and, in response to said detection, de-asserts said first disable signal after a first delay period suitable to allow a clock pulse propagating through said first clock control circuit to be completely output at said selected clock signal.

3. (Currently Amended) The clock selection circuit as set forth in Claim 2 wherein ~~said a first clock control circuit comprises~~:

the first and second flip-flops and the second OR gate in the first clock control circuit form a first clock enable circuit that receives said second disable signal and said first start signal and outputs a first clock enable signal when said first start signal is asserted and said second disable signal is not asserted; and

the first clock control circuit further comprises a first AND gate having a first input coupled to said first clock enable signal and a second input coupled to said first input clock signal, wherein said first AND gate outputs said first gated clock signal.

4. (Currently Amended) The clock selection circuit as set forth in Claim 3 wherein said first clock enable circuit further comprises a first input logic circuit having an output that outputs a Logic 1 when said first start signal is asserted and said second disable signal is not asserted.

5. (Currently Amended) The clock selection circuit as set forth in Claim 4 wherein the first flop-flop has ~~said first clock enable circuit further comprises a first flip-flop having~~ an input coupled to said output of said first input logic circuit, wherein said first flip-flop is clocked by a rising edge of said first input clock signal and said first interlock circuit monitors [[an]] the output of said first flip-flop to detect when said first clock control circuit begins outputting said first gated clock signal.

6. (Currently Amended) The clock selection circuit as set forth in Claim 5 wherein ~~said first clock enable circuit further comprises~~:

the [[a]] second flip-flop has ~~having~~ an input coupled to said output of said first flip flop, wherein said second flip-flop is clocked by a falling edge of said first input clock signal; and

~~a second OR gate having a first input coupled to said output of said first flip-flop and a second input coupled to an output of said second flip-flop, wherein~~ an output of said second OR gate comprises said first clock enable signal.

7. (Original) The clock selection circuit as set forth in Claim 6 wherein said second interlock circuit detects when said second clock control circuit stops outputting said second gated clock signal and, in response to said detection, de-asserts said second disable signal after a delay period suitable to allow a clock pulse propagating through said second clock control circuit to be completely output at said selected clock signal.

8. (Currently Amended) The clock selection circuit as set forth in Claim 7 wherein said [[a]] second clock control circuit comprises:

a second clock enable circuit that receives said first disable signal and said second start signal and outputs a second clock enable signal when said second start signal is asserted and said first disable signal is not asserted; and

a second AND gate having a first input coupled to said second clock enable signal and a second input coupled to said second input clock signal, wherein said second AND gate outputs said second gated clock signal.

9. (Original) The clock selection circuit as set forth in Claim 8 wherein said second clock enable circuit comprises a second input logic circuit having an output that outputs a Logic 1 when said second start signal is asserted and said first disable signal is not asserted.

10. (Original) The clock selection circuit as set forth in Claim 9 wherein said second clock enable circuit further comprises:

a third flip-flop having an input coupled to said output of said second input logic circuit, wherein said third flip-flop is clocked by a rising edge of said second input clock signal and said second interlock circuit monitors an output of said third flip-flop to detect when said second clock control circuit begins outputting said second gated clock signal;

a fourth flip-flop having an input coupled to said output of third flip-flop, wherein said fourth flip-flop is clocked by a falling edge of said second input clock signal; and

a third OR gate having a first input coupled to said output of said third flip-flop and a second input coupled to an output of said fourth flip-flop, wherein an output of said third OR gate comprises said second clock enable signal.

11. (Currently Amended) A processing system comprising:

a clocked circuit capable of operating at a plurality of clock frequencies;

a first clock signal source;

a second clock signal source; and

a clock selection circuit capable of receiving a first input clock signal from said first clock signal source and a second input clock signal from said second clock signal source and outputting to said clocked circuit a selected clock signal derived from one of said first and second input clock signals, said clock selection circuit comprising:

a first clock control circuit that receives said first input clock signal and a first start signal, wherein said first start signal, when asserted, is capable of causing said first clock control circuit to output a first gated clock signal;

a second clock control circuit that receives said second input clock signal and a second start signal, wherein said second start signal, when asserted, is capable of causing said second clock control circuit to output a second gated clock signal;

a first interlock circuit that detects when said first clock control circuit begins outputting said first gated clock signal and, in response to said detection, that asserts a first disable signal capable of preventing said second clock control circuit from outputting said second gated clock signal;

a second interlock circuit that detects when said second clock control circuit begins outputting said second gated clock signal and, in response to said detection, that asserts a second disable signal capable of preventing said first clock control circuit from outputting said

first gated clock signal; and

a first OR gate that receives said first and second gate clock signal and outputs said selected clock signal;

wherein the first clock control circuit comprises a first flip-flop, a second flip-flop coupled in series with the first flip-flop, and a second OR gate having a first input coupled to an output of the first flip-flop and a second input coupled to an output of the second flip-flop.

12. (Original) The processing system as set forth in Claim 11 wherein said first interlock circuit detects when said first clock control circuit stops outputting said first gated clock signal and, in response to said detection, de-asserts said first disable signal after a first delay period suitable to allow a clock pulse propagating through said first clock control circuit to be completely output at said selected clock signal.

13. (Currently Amended) The processing system as set forth in Claim 12 wherein ~~said a first clock control circuit comprises~~:

the first and second flip-flops and the second OR gate in the first clock control circuit form a first clock enable circuit that receives said second disable signal and said first start signal and outputs a first clock enable signal when said first start signal is asserted and said second disable signal is not asserted; and

the first clock control circuit further comprises a first AND gate having a first input coupled to said first clock enable signal and a second input coupled to said first input clock signal, wherein said first AND gate outputs said first gated clock signal.

14. (Currently Amended) The processing system as set forth in Claim 13 wherein said first clock enable circuit further comprises a first input logic circuit having an output that outputs a Logic 1 when said first start signal is asserted and said second disable signal is not asserted.

15. (Currently Amended) The processing system as set forth in Claim 14 wherein the first flop-flop has ~~said first clock enable circuit further comprises a first flip-flop having~~ an input coupled to said output of said first input logic circuit, wherein said first flip-flop is clocked by a rising edge of said first input clock signal and said first interlock circuit monitors [[an]] the output of said first flip-flop to detect when said first clock control circuit begins outputting said first gated clock signal.

16. (Currently Amended) The processing system as set forth in Claim 15 wherein ~~said first clock enable circuit further comprises~~:

the [[a]] second flip-flop in the first clock enable circuit has ~~having~~ an input coupled to said output of said first flip flop, wherein said second flip-flop is clocked by a falling edge of said first input clock signal; and

~~a second OR gate having a first input coupled to said output of said first flip-flop and a second input coupled to an output of said second flip-flop, wherein~~ an output of said second OR gate comprises said first clock enable signal.

17. (Original) The processing system as set forth in Claim 16 wherein said second interlock circuit detects when said second clock control circuit stops outputting said second gated clock signal and, in response to said detection, de-asserts said second disable signal after a delay period suitable to allow a clock pulse propagating through said second clock control circuit to be completely output at said selected clock signal.

18. (Currently Amended) The processing system as set forth in Claim 17 wherein said [[a]] second clock control circuit comprises:

a second clock enable circuit that receives said first disable signal and said second start signal and outputs a second clock enable signal when said second start signal is asserted and said first disable signal is not asserted; and

a second AND gate having a first input coupled to said second clock enable signal and a second input coupled to said second input clock signal, wherein said second AND gate outputs said second gated clock signal.

19. (Original) The processing system as set forth in Claim 18 wherein said second clock enable circuit comprises a second input logic circuit having an output that outputs a Logic 1 when said second start signal is asserted and said first disable signal is not asserted.

20. (Original) The processing system as set forth in Claim 19 wherein said second clock enable circuit further comprises:

a third flip-flop having an input coupled to said output of said second input logic circuit, wherein said third flip-flop is clocked by a rising edge of said second input clock signal and said second interlock circuit monitors an output of said third flip-flop to detect when said second clock control circuit begins outputting said second gated clock signal;

a fourth flip-flop having an input coupled to said output of third flip-flop, wherein said fourth flip-flop is clocked by a falling edge of said second input clock signal; and

a third OR gate having a first input coupled to said output of said third flip-flop and a second input coupled to an output of said fourth flip-flop, wherein an output of said third OR gate comprises said second clock enable signal.